

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-2 and 4-30 are pending. Claims 1-2 and 4-30 stand rejected.

Claims 1, 15, and 23 have been amended. Claim 4 has been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

Applicant reserves the rights with respect to the applicability of the Doctrine of Equivalents.

CLAIM OBJECTIONS

Claim 4 is objected to because of the informality that it depends on a cancelled claim.

Applicants have canceled claim 4.

REJECTIONS UNDER 35 U.S.C. § 103

The Examiner has rejected claims 1-2 and 4-30 under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 6,314,546 to Muddu ("Muddu") in view of U.S. Patent No. 6,601,223 to Puri et al. ("Puri").

Applicants have amended claim 1 to include determining a test network having second electrical characteristics such that the first electrical characteristics of the interconnection are approximated by the second electrical characteristics of the test network within a specified tolerance, wherein determining the test network includes adjusting the second characteristics based on the first graphical representation, wherein the determining includes creating a second

graphical representation of an output of the test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance.

The Examiner stated that “Muddu does not teach approximating by second electrical characteristics of the test network within a specified tolerance” (Office Action, page 4, 10/18/2006). The Examiner contends, however that “ ...Puri teaches the determining includes creating a second graphical representation of an output of the test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance.” (Office Action, page 5, 10/18/2006).

Puri, in fact, discloses estimating interconnect delay through interactive calculations of effective capacitance. More specifically, the Examiner reference to Puri (**Figure 4**) rather discloses the input waveform and the output waveform of the RC circuit. In particular, Puri discloses estimating the output slew of the output waveform from the input slew of the input waveform of the same RC circuit (col. 7, lines 59-66, **Figure 4**). In contrast, amended claim 1 refers to creating a second graphical representation of an output of the test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance.

Muddi, in contrast, discloses an non-iterative approach for estimating interconnect capacitance (Abstract), and similarly to Puri, fails to disclose such limitations of amended claim 1.

Thus, neither Puri, Muddi, nor a combination thereof, discloses creating a second graphical representation of an output of the test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance, as recited in amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. §103(a) over Muddi, in view of Puri.

Given that claims 2, and 5-30 contain similar limitations, applicants respectfully submit that claims 2, and 5-30 are not obvious under 35 U.S.C. §103(a) over Muddi, in view of Puri.


CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact Tatiana Rossin at (408)-720-8300. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

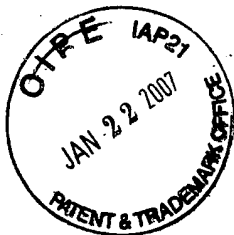
Respectfully submitted,

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Date: 01/18/2007

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Judy L. Steinkraus
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1/18/2007

Application No.: 09/982,242		Filing Date: 10/16/2001	Docket No.: 42P11916X
Date Mailed: 01/18/2007		Due Date: 01/18/2007	
Client: Intel Corporation		Atty/Sec: MJM TVR jxs	
Title: METHOD AND APPARATUS TO EMULATE EXTERNAL IO INTERCONNECTION			
First Named Inventor: Canagasaby			
<u>The following has been received in the U.S.P.T.O. on the date stamped hereon:</u>			
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